CLAIMS

What is claimed is:

1.   A programmable device comprising:

a processing core;

an internal configuration access port coupled to the processing core; and

a plurality of configuration memory cells coupled to the internal configuration access port;

wherein the processing core is configured to access a first subset of the plurality of configuration memory cells as read/write memory.

2.   The programmable device of Claim 1, wherein the first subset of the plurality of configuration memory cells is a don't care set.

3.   The programmable device of Claim 1, further comprising a plurality of unused configurable logic blocks, wherein the first subset of the plurality of configuration memory cells includes configuration memory cells associated with the unused configurable logic blocks.

4.   The programmable device of Claim 1, further comprising a partially configured configuration logic block, wherein the first subset of the plurality of configuration memory cells includes configuration memory cells associated with the partially configured configurable logic block.

5.   The programmable device of Claim 1, further comprising at least one configured logic circuit, wherein the first subset of the plurality of configuration memory

cells excludes configuration memory cells associated with the at least one configured logic circuit.

6.   The programmable device of Claim 1, further comprising a memory management unit coupled between the processing core and the internal configuration access port.

7.   The programmable device of Claim 6, wherein the memory management unit allows random access of the first subset of the plurality of configuration memory cells.

8.   The programmable device of Claim 6, wherein the memory management unit maps the first subset of the plurality of configuration memory cells into a memory map of the processing core.

9.   The programmable device of Claim 1, wherein a second subset of the plurality of configuration memory cells is configured with predetermined user data.

10.   The programmable device of Claim 9, wherein the processing core is configured to access the second subset of the plurality of configuration memory cells as read-only memory.

11.   A programmable device, comprising
        a configured logic circuit;
        an internal configuration access port coupled to
the configured logic circuit; and
        a plurality of configuration memory cells coupled
to the internal configuration access port;
        wherein the configured logic circuit is
configured to access a subset of the plurality of

configuration memory cells containing predetermined user data.

12. The programmable device of Claim 11, wherein the subset of the plurality of configuration memory cells is a don't care set.

13. The programmable device of Claim 11, further comprising a plurality of unused configurable logic blocks, wherein the subset of the plurality of configuration memory cells includes configuration memory cells associated with the unused configurable logic blocks.

14. The programmable device of Claim 11, further comprising a partially configured configuration logic block, wherein the subset of the plurality of configuration memory cells includes configuration memory cells associated with the partially configured configurable logic block.

15. The programmable device of Claim 11, further comprising a second configured logic circuit, wherein the subset of the plurality of configuration memory cells excludes configuration memory cells associated with the second configured logic circuit.

16. The programmable device of Claim 11, wherein the predetermined user data is written into the programmable device in a configuration bitstream that configured the configured logic circuit.

17. The programmable device of Claim 11, wherein the subset of the plurality of configuration memory cells is read-only memory to the configured logic circuit.

18. The programmable device of Claim 11, wherein the configured logic circuit is a processing core.

19. A method of operating a programmable device having a plurality of configuration memory cells and a processing core, the method comprising:

defining a don't care set of configuration memory cells in the plurality of configuration memory cells; and

using the don't care set of configuration memory cells as read/write memory for the processing core.

20. The method of operating a programmable device of Claim 19, further comprising configuring a portion of the programmable device as the processing core.

21. The method of operating a programmable device of Claim 19, wherein the don't care set of configuration memory cells includes configuration memory cells associated with an unused portion of the programmable device.

22. The method of operating a programmable device of Claim 19, wherein the don't care set of configuration memory cells includes configuration memory cells associated with a partially configured configurable logic block.

23. The method of operating a programmable device of Claim 19, further comprising configuring a portion of the programmable device as a memory management unit.

24. The method of operating a programmable device of Claim 19, wherein the defining the don't care set of configuration memory cells comprises:

defining a care set of configuration memory cells; and

defining configuration memory cells not included in the care set of configuration memory cells as the don't care set of configuration memory cells.

25. The method of operating a programmable device of Claim 19, wherein the using the don't care set of configuration memory cells as read/write memory for the processing core further comprises:

reading a frame of data from the don't care set of configuration memory cells;

modifying a portion of the frame of data; and

writing the frame of data to the don't care set of configuration memory cells.

26. The method of operating a programmable device of Claim 19, further comprising storing predetermined user data in a subset of the don't care set of configuration memory cells.

27. The method of operating a programmable device of Claim 26, wherein the storing predetermined user data in the subset of the don't care set of configuration memory cells comprises writing the predetermined user data into the subset of the don't care set of configuration memory cells from a configuration bitstream.

28. The method of operating a programmable device of Claim 26, wherein the subset of the don't care set of configuration memory cells is treated as read-only memory.

17

29.   A method of operating a programmable device
having a plurality of configuration memory cells and a
processing core, the method comprising:

defining a don't care set of configuration memory
cells in the plurality of configuration memory cells;
and

storing predetermined user data in a subset of
the don't care set of configuration memory cells.

30.   The method of operating a programmable device of
Claim 29, further comprising configuring a portion of the
programmable device as the processing core.

31.   The method of operating a programmable device of
Claim 29, wherein the don't care set of configuration
memory cells includes configuration memory cells associated
with an unused portion of the programmable device.

32.   The method of operating a programmable device of
Claim 29, wherein the don't care set of configuration
memory cells includes configuration memory cells associated
with a partially configured configurable logic block.

33.   The method of operating a programmable device of
Claim 29, wherein the defining the don't care set of
configuration memory cells comprises:

defining a care set of configuration memory
cells; and

defining configuration memory cells not included
in the care set of configuration memory cells as the
don't care set of configuration memory cells.

34. The method of operating a programmable device of Claim 29, wherein the storing predetermined user data in the subset of the don't care set of configuration memory cells comprises writing the predetermined user data into the subset of the don't care set of configuration memory cells from a configuration bitstream.

35. The method of operating a programmable device of Claim 29, wherein the subset of the don't care set of configuration memory cells is treated as read-only memory.